REMARKS

Present Status of the Application

The drawings are objected under 37 CFR 1.83(a). The Specification and claims 2, 5, 6, 8, and 10 are objected to because of some informalities. The claims 2, 6 and 8 are rejected under 35U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action rejected all presently-pending claims 1-11. Specifically, the Office Action rejected claim 1 under 35 U.S.C. 102(b), as being anticipated by Iknaian et al. (U.S. Patent No.5,198,758, "Iknaian" hereinafter). The Office Action also rejected claims 2-5 under 35 U.S.C. 102(b) as being unpatentable over Crouch (U.S. Patent No.5,592,493, "Crouch" hereinafter). The Office Action rejected claims 6-11 under 35 U.S.C. 103(a), as being anticipated by Crouch and further in view of Shacham et al. (U.S. Patent No.6,493,840, "Shacham" hereinafter). Applicants have amended a drawing and the specification to overcome the objection and have amended claims 2, 5, 6, 8, and 10 to improve clarity. After entry of the foregoing amendments, claims 1-11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of objections

According to the OFFICE ACTION, the drawings were objected under 37 CFR 1.83(a) because the drawings do not show the "Select" line label as described in the specification. In response thereto, a "Select" line label 419 is added in FIG.4 for indicating that the multiplexing finite state machine controller 418 outputs a select signal 419 to the select input terminal of the multiplexer controller 404, which is supported in Paragraph [0028]. Regarding with the objection of informalities to claims, claims 2, 5, 6, 8, and 10 are amended to improve clarity.

According to the OFFICE ACTION, the claims 2, 6 and 8 are rejected under 35U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response thereto, the misspelled word "multiplexing" has been corrected. Reconsideration of the above objections is thus respectfully requested.

Discussion of Office Action Rejection by the Ikanaian

The Office Action rejected claim 1 under 35 U.S.C. 102(b), as being anticipated by Iknaian. Applicants respectfully traverse the rejections for at least the reasons set forth below.

The invention relates to a method and a circuit of testing a chip which comprises an intellectual product circuit module. A plurality of registers is sequentially configured with a test pattern according to different states. After all of the registers are configured with the test pattern, in a next following state, a test activating signal is sent to the intellectual product circuit module for operation of testing.

The Iknaian reference does not disclose "**sequentially configuring a plurality of registers with the test pattern in a plurality of different states according to the test pattern**" and "**after all of the registers are configured with the test pattern, providing a test activating signal to the intellectual product circuit module in a next state, so that the intellectual product circuit module operates according to the test pattern from the registers**", as defined in amended claim 1.

As disclosed in the Abstract of the Iknaian reference, it is stated as follows:

> A state machine clears the measurement latch, and then loads a test pattern into the test register. **As each bit of the register is set, a corresponding bit in the measurement latch is also set to simulate a measurement cycle**; the results of the "measurement" are stored in the measurement latch. Once the test pattern is loaded, the repeater chip is placed into a measurement test mode. Execution of a measurement test cycle then propagates the test pattern throughout the clock delay path of the regulator. An output clock signal is sampled and if determined present, indicates that the clock path column under

test is functional. Each column of the clock path is then tested separately in sequence",

In the Iknaian reference, the test registers are **shift registers** and are sequentially tested, which is totally different from the invention, in which when all of the registers are configured with the test pattern, a test activating signal is issued to the intellectual product circuit module in a next state so that the intellectual product circuit module begins to test the test pattern in the registers.

For at least the reasons, Applicant respectfully submits that amended claim 1 is not anticipated by the Iknaian reference and is patently defined over the prior art references, and should be allowed.

Discussion of Office Action Rejection by the Crouch and Shacham

The Office Action also rejected claims 2-5 under 35 U.S.C. 102(b) as being unpatentable over Crouch. The Office Action rejected claims 6-11 under 35 U.S.C. 103(a), as being anticipated by Crouch and further in view of Shacham. Applicants respectfully traverse the rejections for at least the reasons set forth below.

The Crouch reference relates to "a serial scan chain architecture for a data processing system and method of operation", which is the same as

disclosed in FIG.1 in the Related Art of the Specification of the invention. As disclosed in the Col.2, Lines 5-14, it stats that "the present invention provides a scan test architecture for use with a full-scan partitioned logic design (a plurality of functional circuit blocks within a single integrated circuit) implementation that is based upon a single serial scan access port with a single scan shift control port and can conduct scan tests at or above the rated frequency of the integrated circuit in such a manner that frequency dependent faults can be detected and isolated within any targeted partition block within the integrated circuit (IC)." The Crouch reference, either along or combined with the Shacham, does not disclose "sequentially configuring a plurality of registers with the test pattern in a plurality of different states according to the test pattern" and "after all of the registers are configured with the test pattern, providing a test activating signal to the intellectual product circuit module in a next state, so that the intellectual product circuit module operates according to the test pattern from the registers", as defined in amended claims 2 and 6.

For at least the foregoing reasons, Applicant respectfully submits that amended claims 2 and 6 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 3, 4, 5, 7, 8, 9, 10 and 11 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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